Claims

What is claimed is:

1. An integrated circuit comprising:

a plurality of digital signal processors, and

a host processor interface coupled to a host processor and to said plurality of digital signal processors.

2. The integrated circuit of Claim 1 further comprising:

a plurality of memory devices, each associated with and coupled to one of said plurality of digital signal processors and each coupled to said host processor interface.

3. The integrated circuit of Claim 2 further comprising:

a common memory bus coupling each of said memory devices to said host processor interface.

4. The integrated circuit of Claim 2 further comprising:

a plurality of direct memory access devices, each associated with one of said plurality of digital signal processors and each coupled to the memory device associated with the respective digital signal processor, and

at least two time division multiplexing devices associate with each digital signal processor and coupled to the direct memory access device associated with each digital signal processor, each time division multiplexing device including a signal port for receiving and sending signals.

5. The integrated circuit of Claim 4 wherein:

each memory device comprises an instruction memory device and a data memory device and each direct memory access device is coupled to a data memory device.

6. The integrated circuit of Claim 5, further comprising:

a common memory bus coupling each of said instruction memory and data memory devices to said host processor interface.

7. The integrated circuit of Claim 1 further comprising an IEEE Standard 1149.1 compliant testing module connected to all digital signal processors on the integrated circuit.

8. An integrated circuit according to Claim 1 wherein:

said digital signal processors comprise ZSP400 digital signal processors.

9. An integrated circuit comprising:

at least two ZSP400 digital signal processors.

10. The integrated circuit of claim 9 further comprising:

a host processor interface coupled to said at least two ZSP400 digital signal processors.

11. The integrated circuit of claim 10 further comprising:

(a) an instruction memory module and controller for and coupled to each digital signal processor;

(b) a data memory module and controller for and coupled to each digital signal processor and to said host processor interface;

(c) a direct memory access device for and coupled to each data memory module; and

(d) at least two time division multiplexing devices for and coupled to each data memory module.

12. The integrated circuit of Claim 11 further comprising:

a common bus coupling each of said instruction memory modules and each of said data memory modules to said host processor interface.

13. The integrated circuit of Claim 9 further comprising:

an IEEE Standard 1149.1 compliant testing module connected to all digital signal processors on the integrated circuit.

14. A method of operating at least two digital signal processors on a single integrated circuit comprising:

coupling said at least two digital signal processors to a host processor using a single host processor interface.

15. A method according to Claim 14 further including:

providing an instruction memory and a data memory for each digital signal processor, and

coupling each instruction memory and data memory to its respective digital signal processor and to said host processor interface.

16. A method according to Claim 15 further including:

using a common memory bus to couple each instruction memory and each data memory to the single host processor interface.

17. The method of claim 14 further comprising:

coupling said digital signal processors to multiple framers by;

(a) coupling one direct memory access device to each digital signal processor;

(b) coupling at least two time division multiplexing devices to each direct memory access device; and

(c) coupling one framer to each time division multiplexing device.

18. The method of claim 15 further comprising:

coupling each direct memory access device to a digital signal processor by coupling a data memory unit to both said direct memory access device and said digital signal processor.

19. The method of Claim 11 wherein:

each of said digital signal processors comprises a ZSP400 digital signal processor.

20. A method of operating at least two ZSP400 digital signal processors on a single integrated circuit comprising:

coupling said ZSP400 digital signal processors to a host processor using a single host processor interface.

21. The method of claim 20 further comprising coupling said ZSP400 digital signal processors to multiple framers by:

(d) coupling one direct memory access device to each digital signal processor;

(e) coupling at least two time division multiplexing devices to each direct memory access device; and

(a) coupling one framer to each time division multiplexing device.

22. The method of claim 21 further comprising:

coupling each direct memory access device to a digital signal processor by coupling a data memory unit to both said direct memory access device and said digital signal processor.